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TRANSMITTAL FORM

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Total Number of Pages in This Submission: 31

Application Number	10/824,016
Filing Date	April 13, 2004
First Named Inventor	Dana Lee and Bomy Chen
Art Unit	2822
Examiner Name	Kiesha L. Rose
Attorney Docket Number	351913-992472

ENCLOSURES *(Check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
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  - ☐ Affidavits/declaration(s)
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- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
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Firm Name	DLA Piper Rudnick Gray Cary US LLP		
Signature	Ronald L. Yin		
Printed name	Ronald L. Yin		
Date	July 6, 2006	Reg. No.	27,607

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FEE TRANSMITTAL for FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($)500.00

Complete If Known	
Application Number	10/824,016
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		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims _____ - 20 or HP = _____ x Fee ($) _____ = Fees Paid ($) _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims _____ - 3 or HP = _____ x Fee ($) _____ = Fees Paid ($) _____

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Multiple Dependent Claims Fee ($) _____ Fee Paid ($) _____

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If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

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SUBMITTED BY

Signature	Ronald L. Yin	Registration No. 27,607 (Attorney/Agent)	Telephone 650-833-2437
Name (Print/Type)	Ronald L. Yin		Date July 10, 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Dana Lee and Bomy Chen

Application No. 10/824,016

Filed: April 13, 2004

For: METHOD OF MANUFACTURING AN ISOLATION-LESS ARRAY OF BI-DIRECTIONAL READ/PROGRAM NON-VOLATILE FLOATING GATE MEMORY CELLS WITH INDEPENDENT CONTROLLABLE CONTROL GATES

Group Art Unit: 2822

Examiner: Rose, Kiesha L.

APPEAL BRIEF

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Control Number: 10/824,016

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July 10, 2006

Kathleen LaBrie

Dear Sir/Madam:

This is a brief for an appeal from a Final Office Action dated February 10, 2006, and from a Notice of Appeal that was filed on May 9, 2006.

TABLE OF CONTENTS

Real Party in Interest

The real party of interest is Silicon Storage Technology, Inc., pursuant to the assignment executed on April 7, 2004, and recorded on April 13, 2004 at reel 015220 and frame 0338.

Related Appeals and Interferences

There are no related appeals or interferences.

Status of Claims

Claims 1-11 were originally presented on the filing of the application. This is an appeal of the rejected Claims 1-11.

Status of Amendments

No amendments were filed subsequent to final rejection.

Summary of Claimed Subject Matter

Applicants' invention, as claimed, deals with a method of making an isolation-less array of non-volatile memory cells in a semiconductor substrate. Specifically, the term "isolation-less" means that no Field Oxide or Shallow Trench Isolation (STI) is used between adjacent rows (or columns) of memory cells. In independent claim 1, the method of making an isolation-less array is disclose in paragraph 2 (hereinafter [0002]), page 1. The semiconductor substrate is shown in Figure 2A as element 20. The step of forming a plurality of spaced apart trenches is shown in Figure 2C as element 28 and is described in [0013], page 4. The step of forming a pair of floating gates in each trench is shown in Figure 2D as element 34 and is described in [0014],

page 4. The step of forming a first terminal is shown in Figure 2D as element 32 and is described in [0017], page 4. The step of forming a control gate is shown in Figure 2E as element 38 and is described in [0018], page 5. The step of forming a conductor on the planar surface is shown in Figure 2G as element 60 and is described in [0020], page 6. The transistors formed are transistors 11 shown in Figure 1 and described in [0019], page 6. The step of patterning is described in [0020], page 6. Finally the step of cutting each pair of floating gates is shown in Figure 2H where element 34 is cut and is described in [0021], page 6.

Grounds of Rejection to be Reviewed on Appeal

The sole ground of rejection to be reviewed on appeal is whether Claims 1-11 were properly rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 6,541,815 ("Mandelman").

Argument

In rejecting claims 1-11, the examiner alleged, without any support, that Mandelman discloses "a conductor (58) on planar surface, which is spaced apart from the planar surface and serves as a gate for a transistor between adjacent transistors." Applicants respectfully disagree.

In Mandelman, the conductor 58 extends over a source/drain region 50 which is in the top planar surface of the substrate. See Fig. 2A. In fact as seen in Figure 2A, the function of the conductor 58 is to be capacitively coupled to the floating gate. As a result, the conductor 58 cannot function as a "gate for a transistor between adjacent trenches", as required by claim 1. Accordingly for at least this reason, the rejection of Claim 1 based upon Mandelman is in error.

Furthermore, with respect to claim 1, claim 1 recites that the control gate which is formed is "continuous in said first direction." For the reasons set forth hereinafter, in response to the

rejection of claim 5, the control gate of Mandelman is not continuous in the first direction. A review of Mandelman shows that the so-called control gate 44 is used only to connect to the word line 60 (see fig. 16B). Thus, contrary to the requirement of Claim 1, the control gate 44 of Mandelman is not continuous in the first direction.

In rejecting claims 3-4 and 10-11, the examiner asserted, without any proof, that Mandelman "teaches that the floating gates are etched and would naturally leave somewhat rounded ends and has a tip along the floating gates at an end closest to the bottom of the trench and tip that is furthest away from the bottom wall."

Applicants respectfully note that Mandelman does not teach either rounding or tipped ends of a floating gate. The floating gates 30 disclosed by Mandleman are substantially rectilinear in shape. See Figure 1, 2A-2C, 7, 8, 9, 10, 11, 12B, 14B, 15B, 16B, and 17B. None of the floating gates 30 shown in any of these figures displays either a rounded end or an end with a tip. Thus, Applicants respectfully traverse this aspect of the rejection.

With respect claim 5, the examiner asserted that Mandelman "teaches the floating gates are etched and the control gates need not be etched. (Columns 7 and 8)" Applicants respectfully traverse this rejection.

A review of Columns 7 and 8 fails to demonstrate that it teaches the etching of the floating gates without etching the control gates. In fact, a review of Figure 15A shows the contrary. The control gate 44 is shown as being disjointed and discontinuous. Therefore, contrary to the examiner's assertion, the control gates appear to be etched at the same time that floating gates are cut. See also Figures 12C and 13 wherein the control gate 44 is not present in those joints. Therefore, the assertion by the examiner is strenuously objected.

Conclusion

For all of the reasons set forth hereinabove, Applicants respectfully submit that the claims appended hereto are patentable and urge a reversal of the final rejection.

Respectfully submitted,

DLA Piper Rudnick Gray Cary US LLP

Dated: July 6, 2006

By: Ronald L. Yin
Ronald L. Yin
Reg. No. 27,607
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Claims Appendix

1. A method of making an isolation-less array of non-volatile memory cells in a semiconductor substrate, having a planar surface; said substrate is of a first conductivity type comprising;

forming a plurality of spaced apart trenches in said planar surface of said substrate in a first direction, each trench having a first sidewall, a second sidewall and a bottom wall;

forming a pair of floating gates along the first and second sidewalls in each trench, each floating gate spaced apart from the first and second sidewalls, respectively;

forming a first terminal of a second conductivity type along the bottom wall of each trench in the substrate;

forming a control gate in each trench; each control gate insulated from and capacitively coupled to the floating gates in the trench and insulated from the first terminal along the bottom wall of the trench, wherein each control gate is continuous in said first direction;

forming a conductor on said planar surface, said conductor spaced apart from said planar surface, wherein said conductor serving as a gate for a transistor between adjacent trenches;

patterning said conductor along a second direction substantially perpendicular to said first direction to form a plurality of spaced apart strips of conductors, with an opening between each pair of conductor strips; and

cutting each pair of floating gates in each trench.

2. The method of claim 1 wherein the step of forming a pair of floating gates comprises:

forming a layer of silicon dioxide along said first sidewall, said second sidewall, and said bottom wall of each trench;

depositing a layer of polysilicon along said silicon dioxide of said first sidewall, said second sidewall and said bottom wall of each trench;

anisotropically etching said layer of polysilicon, to remove said layer of polysilicon from said bottom wall, forming a pair of polysilicon floating gate spacers along the first and second sidewalls in each trench.

3. The method of claim 2 further comprising the step of forming a tip along each of said floating gates at an end closest to said bottom wall in each trench.

4. The method of claim 2 further comprising the step of forming a tip along each of said floating gates at an end furthest away from said bottom wall in each trench.

5. The method of claim 1 wherein said cutting step cuts each pair of floating gates through said opening in each trench without cutting the control gate.

6. The method of claim 2, wherein said step of forming a plurality of spaced apart trenches in said planar surface further comprises:

applying a layer of masking material on said planar surface of said substrate;

patterning said masking material in said first direction to form a plurality of masking strips and a plurality of first openings with a first opening between each pair of masking strips;

etching said substrate to form said plurality of trenches through said first openings.

7. The method of claim 6 wherein the masking material is silicon nitride.

8. The method of claim 1 wherein said cutting step is performed prior to said control gate being formed in each trench.

9. The method of claim 8 wherein the step of forming a pair of floating gates comprises:

forming a layer of silicon dioxide along said first sidewall, said second sidewall, and said bottom wall of each trench;

depositing a layer of polysilicon along said silicon dioxide of said first sidewall, said second sidewall and said bottom wall of each trench;

anisotropically etching said layer of polysilicon, to remove said layer of polysilicon from said bottom wall, forming a pair of polysilicon floating gate spacers along the first and second sidewalls in each trench.

10. The method of claim 9 further comprising the step of forming a tip along each of said floating gates at an end closest to said bottom wall in each trench.

11. The method of claim 9 further comprising the step of forming a tip along each of said floating gates at an end furthest away from said bottom wall in each trench.